REMARKS

In the Office Action[1], the Examiner rejected claims 1 and 5 under 35 U.S.C. § 112, second paragraph; rejected claims 1-6, 11, and 12 under 35 U.S.C. § 103(a) as being unpatentable over Negishi et al. (U.S. Patent No. 6,005,590) ("*Negishi*") in view Inoue et al. (U.S. Patent No. 5,982,380) ("*Inoue*"); rejected claims 7 and 8 under 35 U.S.C. § 103(a) as being unpatentable over *Negishi*, in view of *Inoue*, and further in view of Koss et al. (U.S. Patent No. 5,720,019) ("*Koss*"); and rejected claims 9 and 10 under 35 U.S.C. § 103(a) as being unpatentable over *Negishi*, in view of *Inoue*, in view of Oliver et al. (U.S. Patent No. 5,313,610) ("*Oliver*"), and further in view of *Koss*.

Claims 1 and 5 have been amended. Claims 1-12 remain pending.

Regarding the rejection of claims 1 and 5 under 35 U.S.C. §112, second paragraph, Applicants have amended claims 1 and 5. Applicants have amended "clip registers cascade connected to an output of said current clip register and able to replace the held data" to recite --clip registers cascade connected to an output of said current clip register for replacing the held data--. It is respectfully submitted that claims 1 and 5 fully meet the requirements of 35 U.S.C. §112, second paragraph. Therefore, Applicants respectfully request reconsideration and withdrawal of the rejection of claims 1 and 5 under 35 U.S.C. §112, second paragraph.

Applicants respectfully traverse the rejection of claims 1-6, 11, and 12 under 35 U.S.C. § 103(a).

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[1] The Office Action contains a number of statements reflecting characterizations of the related art and the claims. Regardless of whether any such statement is identified herein, Applicants decline to automatically subscribe to any statement or characterization in the Office Action.

Independent claim 1 recites a clipping device including, for example:

> a clip code generation circuit . . .
> a current clip register for shifting the clip codes generated at said clip code generation circuit;
> clip registers cascade connected to an output of said current clip register for replacing the held data with the clip codes held by the register of a previous stage;

The prior art cited by the Examiner, *Negishi* in view of *Inoue*, does not teach or suggest each and every element of independent claim 1. A *prima facie* case of obviousness has, therefore, not been established.

Negishi discloses, "a clip code indicates if an object is positioned inside or outside a clip space of a rectangular parallelopiped which is defined by clip frames of six chip plates (X=XMAX, X=XMIN, Y=YMAX, Y=YMIN, Z=ZMAX, Z=ZMIN)" (column 7, line 67 - column 8, line 4). Shift registers 304, 305, and 306 hold clip codes for the three vertices and the data from these registers is loaded to the clip state generator 307 and the clip code register 308 (col. 8, lines 53-55).

The Examiner asserts that clip registers 304-306 "constitute 'clip registers cascade connected' as recited above, and the clip code register 308 would then constitute 'clip registers' as recited above" (Office Action at page 5). Applicants respectfully disagree.

Clip code register 308 cannot correspond to the claimed "current clip register" at least because shift registers 304-306, which allegedly correspond to the claimed "clip registers cascade connected," are not "connected to an output of said current clip register," as recited in claim 1. Fig. 3 of *Negishi* depicts clip code register 308

connected to an output of shift registers 304-306. Shift registers 304-306 are not connected to an output of clip code register 308.

In addition, "[a]fter the shift registers 304, 305, and 306 shift their fields, the generated clip codes for the second vertex are loaded to the respective shift registers 304, 305, and 306, and the clip state code 308 generates a clip state code" (col. 9, lines 30-34). Shift registers 304, 305, and 306 have parallel outputs connected to clip code register 308. Because the output of each shift register is loaded to the clip code register 308, there is no output from one shift register to another. Shift registers 304, 305, and 306 are not connected to each other. The output of each shift register is only connected to clip code register 308. Therefore, *Negishi* does not teach or suggest the claimed "current clip register for shifting the clip codes generated at said clip code generation circuit" and "clip registers cascade connected to an output of said current clip register for replacing the held data with the clip codes held by the register of a previous stage," as recited in claim 1.

Inoue does not cure the deficiencies of *Negishi*. *Inoue* discloses a "clipping device for presenting an object to be displayed in a display area" (col. 2, lines 19-20). The Examiner asserts that register 23 corresponds to the claimed "current clip register" and latches 251-253 correspond to the claimed "clip registers cascade connected." Applicants respectfully disagree.

Register 23 "has six registers 231 to 236, and the registers 231, 233 and 235 receives the output S and the registers 232, 234 and 236 receives the output L" (col. 5, lines 35-37). *Inoue* does not teach that register 23 shifts clip codes. Therefore, *Inoue*

does not teach or suggest the claimed "current clip register for shifting the clip codes generated at said clip code generation circuit," as recited in claim 1.

Moreover, latches 251-253 "are connected in series and a shift signal WES controls input/output of data. When the shift signal WES is activated, data stored in the latches 251 to 253 are shifted in this order" (col. 8, lines 11-14 and Fig. 6). Data stored in the latches may be shifted. However, this does not teach or suggest the claimed "cascade." Shifting data within a latch does not teach or suggest the claimed "clip registers cascade connected to an output of said current clip register for replacing the held data with the clip codes held by the register of a previous stage," as recited in claim 1.

Accordingly, *Negishi* and *Inoue* fail to establish a *prima facie* case of obviousness with respect to claim 1, at least because the references fail to teach each and every element of the claim. Claims 2-4 depend from claim 1 and are thus also allowable over *Negishi* and *Inoue*, for at least the same reasons as claim 1.

Independent claim 5, though of different scope from claim 1, recites limitations similar to those set forth above with respect to claim 1. Claim 5 is therefore allowable for at least the reasons presented above. Claims 6, 11, and 12 depend from claim 5 and are thus also allowable over *Negishi* and *Inoue*, for at least the same reasons as claim 5.

Applicants respectfully traverse the rejection of claims 7 and 8, dependent from claim 5. The Examiner relies on *Koss* for allegedly teaching a control circuit that "generates a vertex ready flag indicating that a quantity of vertex of clip codes of said primitive are ready at the time of execution of the replacement instruction" (Office Action

at pages 20-21). Even assuming this assertion is true, *Koss* fails to cure the deficiencies of *Negishi* and *Inoue* discussed above. *Koss* discloses vertex clip code shift registers 220, 244, 246, and 248 (Fig. 4). First vertex clip code shift register 220 includes a series of six single-bit memory cells 232 (323 in Figure 4), 234, 236, 238, 240, and 242 (col. 9, lines 52-55). These memory cells shift their contents by two elements and perform a two-bit parallel load at the same time (col. 10, lines 1-4). For example, the contents of the first memory cell 232 are shifted to the third memory cell 236, and contents from the second memory cell 234 are shifted to the fourth memory cell 238 (col. 10, lines 4-8).

Even assuming, absent any teaching in *Koss*, that the shifting of the contents to different memory cells is a cascade, this cascade only exists within the specific shift register. There is no cascade of the contents between shift registers (See Fig. 4 and 7 of *Koss*). Therefore, *Koss* does not teach "clip registers cascade connected to an output of said current clip register," as recited in claim 1.

Moreover, in *Koss*, "shift registers 220, 244, 246, and 248 have parallel outputs operatively connected to different inputs of an accept/reject circuit 250" (col. 10, lines 18-20). Because the output of each shift register 220, 244, 246, and 248 is fed to the accept/reject circuit 250, there is no output from one shift register to another. No shift registers are connected to each other. As shown in Fig. 4, maximum output line 210 and minimum output line 212 are connected to a respective parallel input line of each of shift registers 220, 244, 246, and 248. The outputs of each shift register is connected to only the accept/reject circuit 250. *Koss* does not teach "clip registers cascade connected to an output of said current clip register for replacing the held data with the

clip codes held by the register of a previous stage," as recited in claim 1. Therefore, claims 7 and 8 are also allowable over *Negishi*, *Inoue*, and *Koss* for at least the same reasons as claim 1.

Applicants respectfully traverse the rejection of claims 9 and 10, dependent from claim 5. Although the Examiner cites *Oliver* in the rejection of dependent claims 9 and 10, Applicants respectfully assert that *Oliver* fails to cure the deficiencies of *Negishi*, *Inoue*, and *Koss* discussed above. Therefore, claims 9 and 10 are also allowable over *Negishi*, *Inoue*, *Koss*, and *Oliver* for at least the same reasons as claim 1.

In view of the foregoing amendments and remarks, Applicants respectfully request reconsideration of the application and withdrawal of the rejections. Pending claims 1-12 are in condition for allowance, and Applicants request a favorable action.

Please grant any extensions of time required to enter this response and charge any additional required fees to our deposit account 06-0916.

Respectfully submitted,

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